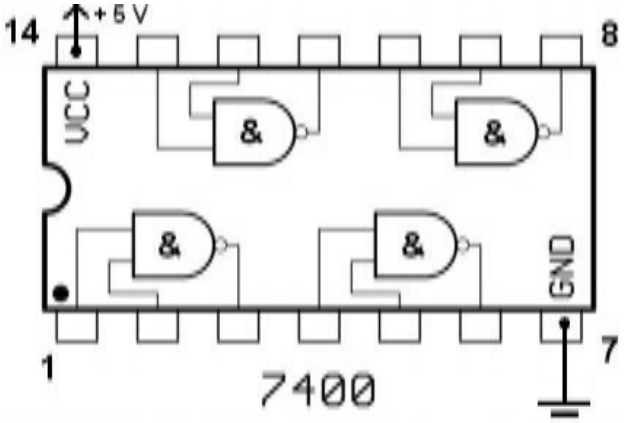
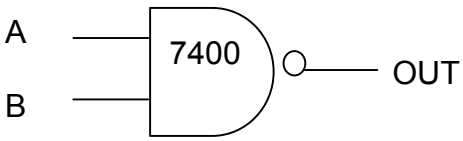
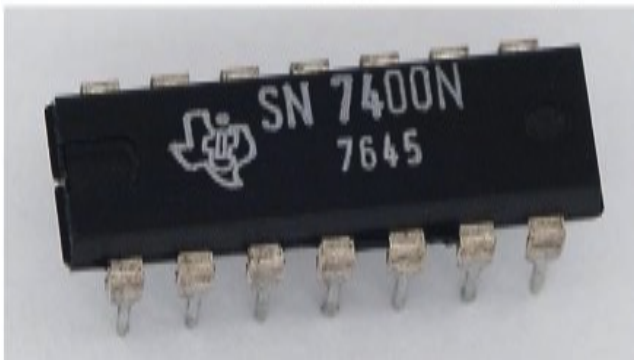
DIGITAL BASICS LAB– 7400/7403 Series

The 7400 series of Transistor-transistor logic integrated circuits are historically important as the first widespread family of TTL integrated circuit logic by Texas Instruments (TI). They were used to build the mini and mainframe computers of the 1960s and 1970s. Several generations of pin-compatible descendants of the original family have since been de-facto standard components.





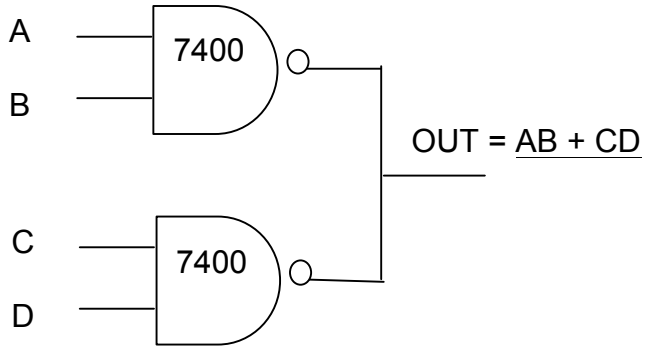


Construct the circuit with an LS7400 2-INPUT POSITIVE NAND GATE. Verify the Truth table. Is it correct?

A	B	OUT
0	0	
1	0	
0	1	
1	1	

WIRED OR GATES

In connecting standard TTL gates by *wired-OR* method to form higher level output logic \the outputs can be fowled up. In our example below when, the output of either 7400 is LO the wired-OR OUT will be shorted to ground. Wire two 7400 gates below.



Answer these with you knowledge of the NAND logic circuit.

1) How many input configs does the NAND circuit have? _____

2) When any input is LO what is the output? OUT = _____

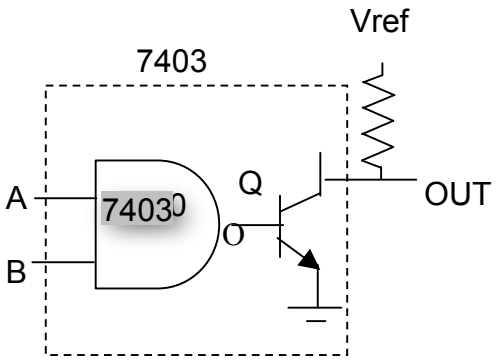
Verify the partial truth table. Is it correct?

A	B	C	D	OUT(theory)	OUT(meas)
0	0	0	0	0+0 = 1	
1	1	1	0	1+0 = 0	
1	1	0	0	1+0 = 0	
1	1	1	1	0+0 = 1	

Comment on the use of the circuit as a 4 input wired NAND. Is the output well defined?

OPEN COLLECTOR NAND

If the output of the standard NAND (other) gate is sent thru a transistor we form the *open collector logic family - 7403*. OUT is attached to a reference voltage Vref through a *pull up resistor*. Any input LO and Output goes HI.



Q	OUT
1	transistor on, I>0, OUT = 0
0	Transistor off, I=0, OUT = Vref

Construct this open-collector NAND circuit fill in the truth table. Measure the Q1 and Q2 outputs with your DMM meter. Is the truth table correct?

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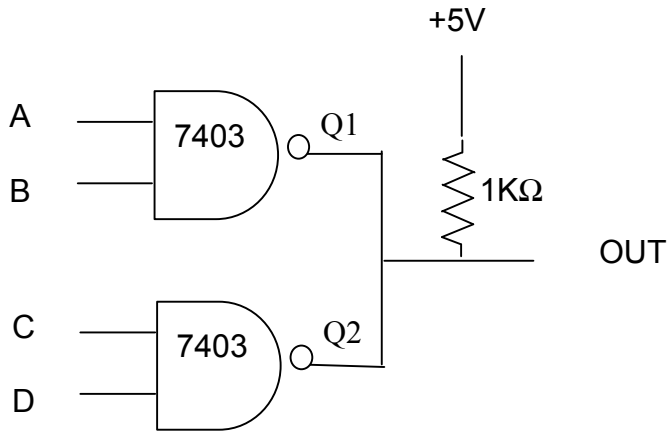

A	B	C	D	Q1	Q2	OUT_{Th}	OUT_{Meas}
0	0	0	0				
1	0	0	0				
1	1	0	0				
1	1	1	1				